REMARKS

This responds to the Office Action mailed on April 9, 2008.

Claims 1, 10, 21, 30, 31, 34, 35 and 38 are amended, no claims are canceled, and no claims are added; as a result, claims 1-32 and 34-38 are now pending in this application.

Specification Objections

The specification has been amended as requested to update the status of the related U.S. applications.

§102 Rejection of the Claims

Claims 1-3, 5-6, 21-23, 25-26, 31-32, 34, 36 and 38 were rejected under 35 U.S.C. § 102(b) for anticipation by Smith, III et al. (US 6,339,813, hereinafter "Smith").

Claim 1, 21, 31, 34 and 38 have been amended to more clearly define Applicant's claimed invention. As amended, claims 1, 21, 31, 34 and 38 relate to a method and computer system for decoupling write addresses from their corresponding write data in a store to a shared memory connected across a network to a plurality of processors. In particular, for example, amended claim 1 recites "transferring a write request to the shared memory, wherein the write request includes the write request address," "when the corresponding write data becomes available, transferring the write data to the shared memory in instruction order across the network without the write request address" and "pairing, within the shared memory, the write request address with the separately transferred corresponding write data." Each independent claim 21, 31, 34 and 38 has similar limitations corresponding to the limitations of claim 1 as cited above.

The Office Action states, at p. 3, #4, that:

> As to claims 1, 21, 31, 34 and 38, Smith discloses in a computer system (Fig. 1) having a plurality of processors (Fig. 1, Refs. 104) connected to **a shared memory (Fig. 1, Ref. 106)** ...; noting the write request address in the shared memory (col. 2, lines 31-44); comparing (col. 2, line 35), in he shared memory, addresses in subsequent load and store requests to the write request address (col. 2, lines 36-39, cache line); transferring the write data to the shared memory (col. 2, lines 36-39); matching (col. 2, lines 35-44, cache

> hit reads on this limitation), within the shared memory, the write request address to its corresponding write data …

As quoted above, the Office Action seems to equate Smith's Level 3 Cache (L3) 106 shared by two processor nodes (104 and 104') to Applicant's shared memory.

Applicant respectfully disagrees. In particular, the relevant portions of Smith state that:

> (Col. 2, lines 16-44) The processors 101 request read or write access to information stored in the nearest caches 102, 103 through a local independent address and data bus (not shown) within the processor node 104 …**If the requested data is found within one of the neighboring processor nodes 104'**, then that node may notify the devices on the bus of the condition and forward the information to the requesting processor directly **without involving the shared cache [i.e., L3 cache] any further. Without such [a] notification**, the shared memory controller 105 L3 cache controller 108 will simultaneously address the shared cache directory 116 and present the DRAM row address cycle on the cache address bus 117 according to the DRAM protocol. In the next cycle, **the [shared cache] directory contents are compared to the request address tag**, and if equal and the cache line is valid (cache hit), then the DRAM column address cycle is driven on the cache address bus 117 the following cycle to read or write access the cache line information. The shared memory controller 105 acknowledges processor read requests with the requested data in the case of a cache hit, otherwise the request is acknowledged to indicate retry or defer to the processor, implying that a cache miss occurred and the information will not be available for several cycles.
>
> (Col. 3, lines 17-25) … **a line fill [to a lower memory level (e.g., the L3 cache)] always involves updating the associated directory entry with the new tag address** and relevant state bits.

As quoted above, Smith checks addresses in the L3 cache first and then "write access the cache line information" at a following cycle. Smith does not, however, show transferring write data corresponding to early checked write addresses in instruction order, eliminating the need for the write data to have an address identifier associating with the write request address. As such, as quoted above, Smith needs to look at the shared cache directory 116 and compare the tag addresses to match the write data to its corresponding write request address.

In contrast, as cited above, amended claims 1, 21, 31, 34 and 38 recite "transferring the write data to the shared memory in instruction order across the network without the write request address" and "pairing, within the shared memory, the write request address with the separately transferred corresponding write data [in the instruction order]." That is, Applicant's claimed invention not only decouples the write data from its corresponding write request address but also

forces ordering in transferring the write data to the shared memory. Since the transferring of the write data is done in instruction order, the Applicant's clamed invention obviates the need to send the write request address again along with the write data. This also allows pairing the early transferred write request address with the separately transferred corresponding write data without comparing the write request address in the shared memory. Nowhere are such teachings as required by amended claims 1, 21, 31, 34 and 38 found in Smith.

For the reasons set forth above, Applicant respectfully submits that Smith fails to show decoupling a write address from its corresponding write data in a store to a share memory as taught by Applicant and claimed in amended claims 1, 21, 31, 34 and 38. Reconsideration and allowance of amended claims 1, 21, 31, 34 and 38 is respectfully requested.

Claims 2, 3, 5, 6, 22, 23, 25, 26, 32 and 36 are allowable as being dependent on one of corresponding independent claims 1, 21, 31 and 34 which are believed to be allowable.

§103 Rejection of the Claims

Claims 4 and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith (US 5,796,980) in vie wof Parks (US 6,356,983).

Claims 7-10, 27-30, 35 and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith, II et al. (US 6,339,813) in view of Handy (Handy, J., The Cache Memory Book, Academic Press, 1993, pp. 73-84.).

Claims 4, 7-10, 24, 27-30, 35 and 37 are allowable as being dependent on one of corresponding independent claims 1, 21 and 34 which are believed to be allowable.

Allowable Subject Matter

Claims 11-20 have been allowed.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6909

Date October 9, 2008 By Thomas J. Brennan
Thomas F. Brennan
Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 9th day of October, 2008.

CANDIS BUENDING
Name

Candis Buending
Signature